



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,810	01/16/2004	Chien-Wei Li	H0003762-1170	8268
7590	07/06/2006			
Honeywell International, Inc. Law Dept. AB2 P.O. Box 2245 Morristown, NJ 07962-9806				EXAMINER PADGETT, MARIANNE L
				ART UNIT 1762 PAPER NUMBER

DATE MAILED: 07/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,810	LI, CHIEN-WEI	
Examiner	Art Unit		
Marianne L. Padgett	1762		

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 1/16/2004 & 5/25/2006.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-49 is/are pending in the application.

4a) Of the above claim(s) 1-35 and 41-49 is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 36-40 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____.
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>1/16/04</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____.

Art Unit: 1762

1. Applicant's election with traverse of group III, method claims 36-40 in the reply filed on 5/25/2006 is acknowledged. The traversal is on the ground(s) that a serious burden has not been established as both groups III & IV are classified in 427/596. This is not found persuasive because: (1) the examiner who made the restriction was not a process examiner and did not get the classification correct. Group III is properly classified in 427/567, while group IV is properly classified in 427/570. The classification of method group V is noted to be appropriate. (2) Furthermore, besides the different deposition techniques between III (electron beam of preparation) & IV (electron beam with plasma), which is reflected their proper classifications, the chemistry & compositions of these two groups is different, such that they constitute totally different searches for Ta₂O₅ on Si-based substrate versus yttria-stabilize zirconium on a Ni superalloy turbine. Hence, even if the processes were claimed the same, or were the same general classification, the search is different, especially as use of the computer for searching essentially restricts one to a word search, if there is no a picture search, such that it is no longer practical/possible in the time allotted, to look through an entire subclass anymore. Thus, searching for two different concepts & combinations of materials, amounts to two separate examinations or a serious burden, before one even does to the rest of the examination.

As an example of added burden, it is noted most of the references in the 1/16/2004 IDS are directed to limitations in nonelected group IV, and have little relevance or used with respect to the electric group, thus the review contributes little to the examination of the elected claims, but takes time.

The requirement is still deemed proper and is therefore made FINAL.

2. With respect to the scope of the claimed "electron beam physical vapor deposition" (EB-PVD), the examiner notes that nowhere in the specification does it appear to describe how the electron beam is intended to be used in the physical vapor deposition process, and the claims especially do not specify, hence would appear to include any technique ~~that~~ employs electron beams anywhere in a PVD

Art Unit: 1762

process, i.e. use of the EB to cause evaporation, or to excite paper by passing the EB through the vapor, or modification of deposit by directing the EB at the deposit on the substrate, etc.

3. Claims 36-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Use of relative terms that lacked clear metes and bounds in the claims, or in a clear definition provided in the original specification or in relevance cited prior art, is vague and indefinite. In independent claims 36, "uniform" is a relative term, whose scope is unclear. What about the layer is intended to be uniform, its composition, its thickness, the area over which it's deposited (i.e. continuous as opposed to discontinuous), etc.?

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 36-38 & 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawashima et al. (5,660,697) in view of Kim et al. (6,486,021 B2), or vice versa.

Kawashima et al. (697) teach deposition of insulating films that may be columnar tantalum pentoxide deposited via plasma CVD or sputtering processes, where it is further taught to improve the deposition process via electron beam heating of the source material (target), with the columnar dielectric crystal layer taught to have a dielectric constant several times higher than used in conventional devices. The substrate on which the deposit takes place is a transparent insulating material, such as glass, with electrodes that may be formed of indium tin oxide formed as a pattern for reality of stripes on the substrate surface over which the tantalum pentoxide insulating layer is deposited. Thereafter, a doped light-

Art Unit: 1762

emitting layer is deposited thereon, another dielectric layer, and then an upper electrode. See the abstract; figures 1 & 4; col. 1, lines 28-34; col. 2, lines 14-33 & 55-col. 3, line 58+, especially lines 3-21 & 54-55; and col. 5. Kawashima et al. differs from the claims by not providing in atomic layer deposition (ALD) deposit on the columnar crystal layer, nor requiring a bond layer (bonding coat) by ALD.

Kim et al. (021) teach making a semiconductor device on which capacitor dielectrics of tantalum pentoxide are deposited on a substrate, whose surface consists of an insulating layer (122) of glass (BPSG), with polysilicon lower electrodes thereon, and a diffusion barrier layer (silicon nitrite) between the polysilicon electrode and the tantalum pentoxide dielectric layer is formed via a thermal nitration process, which has a surface treatment may be considered to read on and ALD process. A composite film, $Ta_{2x}Al_{2(1-x)}O_y$, is deposited via ALD over the Ta pentoxide, followed by upper electrode deposit. See the abstract; figures; col. 1, line 61-col. to lines 20 & 63-col. 4, line 39+, especially col. 3, lines 1-11, 29-42 & 64-67+. Kim et al. teaches the importance of incorporating high K. dielectrics as the capacitor dielectrics film, noting that tantalum pentoxide grown with columnar structure have been known for use as such, but are difficult to apply, or that alternately multilayer dielectrics including tantalum oxides have been employed (col. 1, lines 8-12 & 32-48). Commit L. proposes several alternate deposition techniques for the high K. tantalum pentoxide, including ALD, thermal or UV oxidation techniques (col. 3, lines 44-63). Kim et al. differs by not requiring the use of in EB vapor deposition process to deposit columnar tantalum pentoxide.

It would have been obvious to one of ordinary skill in the art to employ the ALD composite layer of Kim et al. in Kawashima et al. in order to correct for/improve upon leakage current problems that are taught by Kim et al. to be potential problems with columnar tantalum pentoxide, but corrected for with Kim et al.'s composite layer combined with a tantalum pentoxide layer, especially considering that both references objectives are to produce high K. dielectric material for analogous uses. Alternately, it would've been obvious to one of ordinary skill in the art to employ the EB assisted vapor deposited high

Art Unit: 1762

K dielectric columnar Ta pentoxide of Kawashima et al. in Kim et al for the high K Ta pentoxide, as Kim et al. presents several alternative means for depositing tantalum pentoxide, does not disclose what if any crystal structure is desired therefore, but does desire the layer to have a high K dielectric constant, such that use of Kawashima's deposition process would have been expected to provide such, with the ALD deposited composite layer expected to correct for potential (but not necessary) high leakage current problems. It is further noted that Kim et al. provides alternate electrode material (polysilicon) that is effective for lower electrodes with high K Ta pentoxide dielectrics, but notes the need for a barrier layer which can be considered equivalent to the claimed bond coat, when polysilicon electrodes are employed, hence it would've been further obvious that one of ordinary skill in the art to employ such alternate electrode materials, as they have been shown to be effective in analogous situations, thus providing useful alternative materials.

6. Alternate reasons for applying barrier and/or bond coatings between electrodes or electrically conductive material on semiconductor substrates and dielectric layers, such as Ta pentoxide, can be seen in Hayashi et al. (3,819,990), who teaches improvement of the properties of a capacitor, when electrode surfaces such as aluminum are oxidized (an ALD like process), thus improving the boundary there between them permitting easier crystallization of the dielectric (abstract; col. 1, line 65-col. 2, line 45, especially 33-45), where Hayashi et al. further notes that it is known to employ a protective layer on the outer surface of the dielectric to reduce current leakage, which is consistent with the teachings of Kim et al., hence Hayashi et al. is considered cumulative to the above rejection, supplying alternative electrode materials with improved bonding procedures. For the claims as presently broadly written, Hayashi et al. is redundant to the above.

Further references noting the need for barrier interface layers due to incompatibility of high K. materials, inclusive of Ta pentoxide include En et al. (6,563,183 B1; abstract; figures 5; col. 5, lines 55-17), where ALD processes may be employed for depositing the interface layer; Hantangady et al.

Art Unit: 1762

(6,335,238 B1; abstract, figures; cols. 2 & 4), who teaches one or two monolayers of silicon carbide as a reaction barrier between semiconductor substrates in tantalum pentoxide high K dielectrics; Chung (2004/0125541 A1), who teaches a dual diffusion barrier ($\text{Al}_2\text{O}_3 + \text{Si}_3\text{N}_4$) between the tantalum pentoxide dielectric in the lower electrode; and Wallace et al. (6,277,681 B1; abstract; figures; col. 2, lines 36-col.3, line 2)

7. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawashima et al. (5,660,697) in view of Kim et al. (6,486,021 B2), or vice versa as applied to claim 36-38 & 40 above, and further in view of Wallace et al. (6,277,681 B1).

The above rejection does not teach the possibility of the inorganic layer being materials, such as silicon carbide or nitride or various oxycarbides, carbonitrides or mixtures and alloys, etc., however Wallace et al. who is also teaching dielectric layers between electrodes, where the electrodes are polysilicon may employ the sequence of two monolayers of silicon nitride, then a higher dielectric constant material such as Ta pentoxide, then another two monolayers of silicon nitride, where the use of silicon nitride is said to minimize prior art problems concerning drive current in the capacitance, thus appears to be employing the silicon nitride layers for reasons analogous to/ compatible with Kim et al.'s composite ALD layer, hence depending on the material employed for the upper electrode it would've been obvious to one of ordinary skill in the art to alternatively employ monolayers (a suggested of ALD processing) silicon nitride over the high K tantalum pentoxide of the above rejection, as it has been shown to be effective employed in analogous circumstances for analogous purposes, providing desirable effects, particularly with use of polysilicon electrode materials, which also may be employed in the above combination.

8. Claims 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taga et al. (5,305,143) in view of Gates et al. (6,203,613 B1).

Art Unit: 1762

Taga et al. teaches substrates (Si or glass) with a matrix of fine columns deposited thereon, which may be EB-vapor deposited Ta pentoxide, on which a light absorbing coating material may be applied, where it is taught to avoid excess deposit of the light absorbing material, as it impairs the transmission and disturbs the crystal orientation. The taught light absorbing materials are inclusive of various inorganic materials, such as metals (Cu, Ag, Au), semiconductors (SnTe, PbSe, PbTe, Si & Ge) & conductive oxides (ITO or ZnO), and may be deposited via vapor deposition techniques. See the Abstract; Figures 6-8, especially 6(f-g) & 8(c), and 9; col.3, lines 20-65; col. 7, lines 19-62; col. 9, lines 24-30 & 60-col. 10, line 8; col. 11, lines 10-55; col.12, lines 1-8, 20-45 (EB evaporation) & 56-68+; col. 13, lines 29-68 , especially lines 50-63; and col. 14, lines 7-24 giving uses & example 1 with an alternative means of supplying the light of absorbed. Primary reference differs from the claims by not requiring this organic layer to be deposited via an ALD process, although the deposition requirements are suggestive of conformal, as they must continuously coat the columnar surface as illustrated. It would've been obvious to one of ordinary skill in the art to employ specific vapor deposition techniques capable of coding as illustrated, while supplying minimal or minimum required thicknesses for the light absorbing material. Gates et al. can be considered to provide such a technique, as it is teaching an ALD process whose coatings have excellent uniformity and is suggested for use in depositing various metal contain films inclusive of metals or metal oxides, where the metal may be Sn, Cu, Al, Si, In, etc., thus would have been expected to be able to deposit materials as desired by Taga et al. for their light absorbing layer, while fulfilling the criteria of the conformation that is required for these films.

9. Other art of interest include the 1985 IBM technical disclosure bulletin & the Japanese patent JP-182,385 to Kawasaki et al., which discussed electron beam vaporization techniques for depositing tantalum oxide onto silicon substrates, with JP 5-47473 to Kawashima and full et al. having similar teachings in its abstract 2US patent 5,660,697 applied above.

Art Unit: 1762

Also of interest are copending applications 10/982,445 & 10/644, 5232 overlapping inventors which concern processes that may deposit tantalum oxide layers with other layers on top, however the tantalum oxide is not required to be columnar, nor are the succeeding layers required to be deposited via ALD. US PN 6,582,779 B2 to Li et al., also has overlapping inventors, is within a year of the filing date, and while it has claims of depositing tantalum pent oxide via EB-evaporation, again there is no requirement of columnar grain structure nor succeeding ALD deposit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marianne L. Padgett whose telephone number is (571) 272-1425. The examiner can normally be reached on M-F from about 8:30 a.m. to 4:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Meeks, can be reached at (571) 272-1423. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MLP/dictation software

6/17-18/2006



MARIANNE PADGETT
PRIMARY EXAMINER